Transient Behavior and Phase Noise Performance of Pulsed-Harmonic Oscillators

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***Abstract*—The analysis of a low-power, temperature- and supply voltage-independent oscillator based on a pulsed LC tank is presented. The frequency is determined by a bondwire inductor and a MiM capacitor to obtain a high-Q LC tank. Due to a novel way of driving the LC tank, the power consumption is reduced. Since the driving technique only interacts with the LC tank during a very short period, the frequency mainly depends on the stable LC tank, hence the temperature and supply voltage dependency is lowered drastically. The phase noise of the tank, the noise propagation and the transient effects of the driving technique are analyzed theoretically. The results are compared to a 130 nm test chip. The samples were measured over a 0.6 to 1.6 V supply range and a −40 to 100°C temperature range showing a very low temperature dependency of 92 ppm/°C and a voltage dependency of 73 ppm/V. The frequency standard deviation over 12 automatically bonded samples of the same wafer is 0.76% (359 KHz).**

***Index Terms*—Impulse sensitivity function, low-power, oscillators, phase noise, pulsed harmonic.**

I. Introduction

In Wireless Sensor Networks (WSN) and Ultra Low Power RFID applications, a need for devices powered by energy scavenging is emerging. As shown in [1] and [2], this results in an unstable supply voltage. To obtain pulsed Ultra Wideband (UWB) communication between the different nodes of the WSN, a power supply and temperature (PVT) stable, low-frequency oscillator is required. Apart from the PVT stability, which for high-Q resonators mainly depends on the tank components, also the power consumption is an important specification in this application. Therefore, instead of using standard harmonic oscillators, one can use a Pulsed-Harmonic topology [3]. Furthermore, as will be demonstrated, the dependency on voltage and temperature dependent transistor parameters is diminished. Indeed, the driving transistors are only active in a small part of the oscillation period. During the remainder of the oscillation period, the LC tank is free-running. The influence of the variation on this pulse as well as the influence of the pulse itself on the frequency are investigated using a numeric oscillator model.

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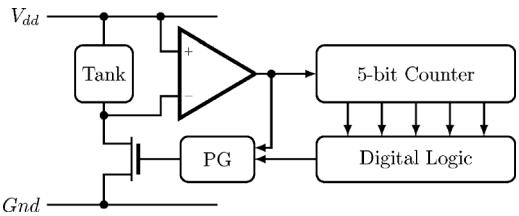

Fig. 1. Block diagram of a pulsed harmonic oscillator. Instead of a negative resistance or g_m, only a NMOS switch is used to drive the tank. PG is the pulse generator.

A possible drawback of this kind of oscillators are the waveform and its impact on the phase noise performance. When only looking at the free-running cycles of the oscillator, the phase noise is mainly determined by the waveform and the tank properties. However, when a pulse is applied to the tank, the oscillation period is affected and a noise portion coming from the pulse generator is injected. The influence of both effects on the low-frequency output is analyzed elaborately.

An integrated high-Q resonant tank can best be obtained by combining a capacitor and an inductor [4]. The temperature and voltage dependency (nonlinearity) of these components is negligible. Integrated inductors, however, suffer from substrate coupling and Eddy currents, which reduce the Q factor drastically. Hence, a bondwire inductor is used instead [5]. The paper is organized as follows. The next section focuses on the possible tank topologies, their transfer function and transient behavior. Next, in Section II.B, the influence of the applied pulses on the frequency of the oscillator is discussed. Sections III and IV discuss the phase noise behavior of a pulsed oscillator. The implemented circuit is discussed in Section V. In Section VI the measurement results are presented and compared to the theoretical results. Conclusions are drawn in Section VII.

II. Transient Behavior of the Pulsed Oscillator

The working principle of a pulsed harmonic oscillator circuit is elaborately described in [3]. Fig. 1 shows a block diagram of a generic pulsed oscillator. The main components of the oscillator are the tank, the amplifier and a counter to count the tank's output periods. After a certain number of cycles, the digital logic activates the pulse generator. The generated pulse is injected in the tank, typically this is done by an NMOS switch. This results in a waveform similar to Fig. 2. Most integrated electronic energy tanks are RC or LC tanks. Other, external, tanks can be based on a ceramic resonator, i.e., a quartz crystal. Here, the focus is on high-Q LC tanks.

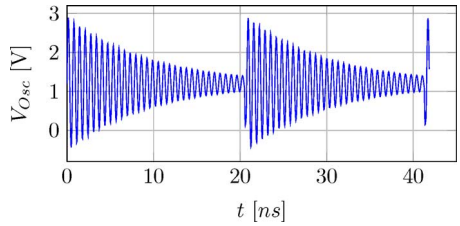

Fig. 2. Simulated waveform of a pulsed LC oscillator. Between pulses the amplitude is decaying due to the losses in the LC tank.

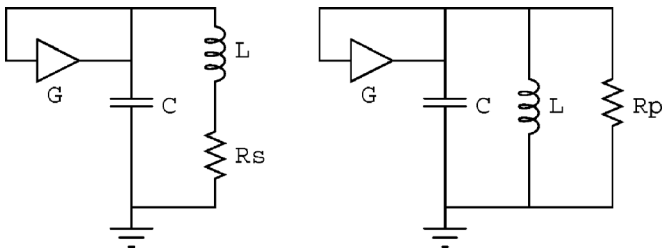

Fig. 3. General schematic of an LC oscillator with a series resistance. On the right, the same LC tank is transformed to a model with parallel resistance. The transconductance amplifier compensates for the losses in R_s or R_p.

A. Second Order LC Tanks

To understand and predict the behavior of the tank, a more detailed study is needed. Since the behavior of a pulsed oscillator is determined by pairs of complex conjugate poles [6], the following discussion is limited to the case of a 2-pole LC system. This system can possibly be part of a higher-order system. LC networks can have, at least in theory, an infinitely high Q factor. Therefore, these resonators are very suitable to build low-noise and low-power oscillators. Series as well as parallel LC networks can be used as a frequency-dependent or tuned network. In the context of this paper, the parallel network shown in Fig. 3 with a series resistor in the inductor is discussed. The current to voltage transfer function of this network is:

$$Z_{\text{eq}} = H(s) = \frac{\frac{s}{C} + \frac{R_s}{L \cdot C}}{s^2 + \frac{R_s}{L} \cdot s + \frac{1}{L \cdot C}} \tag{1}$$

$$= \frac{\omega_n \cdot \sqrt{\frac{L}{C}} \cdot s + \omega_n^2 \cdot R_s}{s^2 + \frac{\omega_n}{Q} \cdot s + \omega_n^2} \tag{2}$$

$$\text{since } Q = \sqrt{\frac{L}{C}} \frac{1}{R_s}$$

$$\text{and } \omega_n = 1/\sqrt{LC} \tag{3}$$

Splitting this function in partial fractions results in:

$$H(s) = \frac{1}{2} \cdot \frac{\omega_n R_s Q \left(1 + \frac{1}{\sqrt{1-4Q^2}}\right)}{s - \frac{-\omega_n \left(1 - \sqrt{1-4Q^2}\right)}{2Q}} \tag{4}$$

$$+ \frac{1}{2} \cdot \frac{\omega_n R_s Q \left(1 - \frac{1}{\sqrt{1-4Q^2}}\right)}{s - \frac{-\omega_n \left(1 + \sqrt{1-4Q^2}\right)}{2Q}} \tag{5}$$

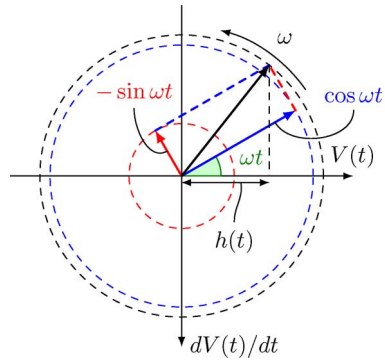

Fig. 4. Phasor diagram of the impulse response. To keep the period constant, a new Dirac impulse must be applied at zero-crossing of the cosine and *not* at the maximum of $h(t)$.

The impulse response contains only one dominant angular frequency equal to:

$$\omega = \omega_n \cdot \sqrt{1 - \frac{1}{4Q^2}} = \sqrt{\frac{1}{\text{LC}} - \frac{R_s^2}{4L^2}} \tag{6}$$

The time constant of the amplitude decay is equal to:

$$\tau = \frac{2Q}{\omega_n} = \frac{2L}{R_s} \tag{7}$$

and is proportional to the oscillation period. This means that the Q factor is a measure of the number of cycles it takes to half the amplitude. Large bondwire inductors can reach a Q factor of 45, resulting in an amplitude decay of a factor of 10 over 32 cycles.

B. Impact of the Applied Pulses

The behavior of a pulsed oscillator is determined by the tank and the pulses applied to the circuit. Since the tank is a linear network, the superposition principle can be applied. This means that, when perturbing the tank with a Dirac impulse every n cycles, the frequency of the oscillator can be kept constant. From (4) it follows that the impulse response of the LC tank is equal to:

$$h(t) = \omega_n R_s Q e^{\frac{-\omega_n}{2Q}t} \left[\cos\left(\frac{\sqrt{4Q^2-1}}{2Q} \omega_n t \right) \right. \tag{8}$$

$$\left. - \frac{\sin\left(\frac{\sqrt{4Q^2-1}}{2Q} \omega_n t \right)}{\sqrt{4Q^2-1}} \right] \tag{9}$$

Since the resulting waveform is a sum of a cosine and a sine, the oscillation does not start at phase 0. The negative sine leads the cosine by $\pi/2$ and represents a small part of the impulse response. This is shown in Fig. 4. The timing of the applied pulses is crucial to avoid jitter in the output signal. Only when a pulse is applied exactly at the $n \cdot 2 \cdot \pi$ crossing of $\omega \cdot t$ (the zero degree crossing of the cosine phasor), the output period stays constant. Only for $Q >> 1$ this moment is equal to the zero

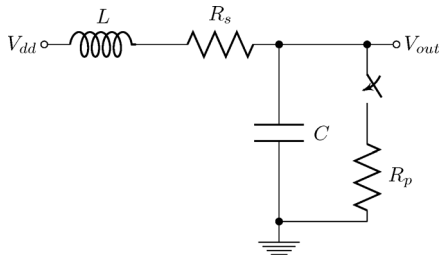

Fig. 5. Schematic model of the tank. This model is numerically simulated in Matlab, the switch is closed (pulsed) once every 32 cycles.

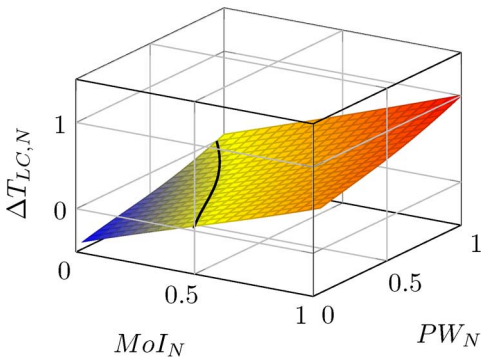

Fig. 6. Impact of a real pulse applied to the network of Fig. 5. When the right combination of pulse width (PW) and moment of impact (MoI) are applied, the time between the zero crossings is not biased (black line). All the values are normalized to half the LC tank oscillation period.

crossing of the resulting output phasor or the maximum of the output voltage.

In a real system, instead of a Dirac impulse, pulses with a finite pulse width will be applied. To simulate this, the RLC-tank was modeled in Matlab. A pulse is applied by connecting a resistor to discharge the tank capacitor once every 32 cycles. The schematic is shown in Fig. 5. For a given tank, the pulses are determined by 3 parameters, which can be controlled independently: the switch resistance R_p, the pulse width PW and the moment of impact MoI. Fig. 6 shows the impact of the pulses at the moment of the next zero crossing as a function of PW and MoI. Also the output amplitude is affected by these two parameters, as shown in Fig. 7. It is observed that by choosing the correct combination of PW and MoI, the timing of the zero crossings is not affected. Fig. 8 shows these optimal combinations for different values of the switch resistance R_p. Note that the case of infinitely short pulses (Dirac impulses, $\mathrm{PW} = 0$) fits with these simulation results. These results can also be obtained analytically, by solving the differential equation of the network for an open and a closed switch. Afterwards, the different regimes can be coupled by their start and stop conditions. The analytical solution to this, however, leads to complex and lengthy expressions, which makes the numerical solution much more straightforward and useful.

Due to the high Q factor of the inductor, the time constant of the capacitor is dominant and the differences for different values of R_s are negligible. This was also expected from Fig. 4 and (9): the size of the sine component is small for a high-Q resonator. The number of free-running cycles and the supply voltage also have no influence on the optimal PW-MoI combinations. This means that, while designing a pulsed LC oscillator, the pulse

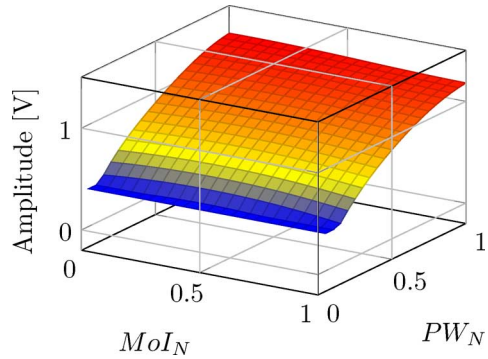

Fig. 7. Oscillation amplitude as a function of the pulse width (PW) and the moment of impact (MoI). A longer pulse leads to a higher amplitude, but also the moment of impact has an influence on the output amplitude of the tank. All the values are normalized to half the LC tank oscillation period.

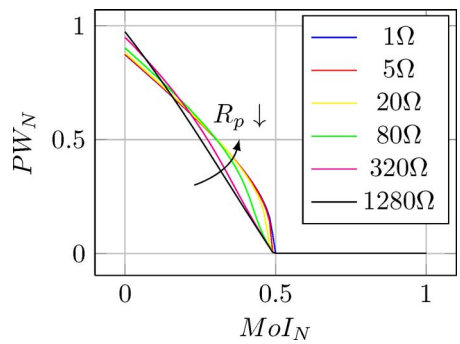

Fig. 8. Optimal length ($\Delta T = 0$) of the applied pulses (PW) as a function of the moment of impact (MoI) for different switch resistances R_p. Both axes are normalized to $T_{\mathrm{LC}}/2$, half the LC tank oscillation period.

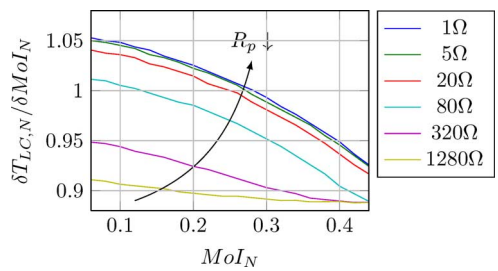

Fig. 9. Sensitivity of the oscillation period to the moment of impact. The derivative is calculated for the optimal PW-MoI combinations. All axes are normalized to half the oscillation period since this is the time span in which the pulse is applied.

generator circuit can be designed independently of these parameters. The optimal combination of PW and MoI, both normalizes to the oscillation period, is a fixed value, independent of the tank properties. This, however, only holds for a constant impedance of the switch, independent of the voltage over the switch. Although an optimal PW-MoI combination can always be found, it is advisable to keep the switch in the linear region to benefit from the described independences.

1) Sensitivity to PW and MoI: When designing the pulse generator, the sensitivity of the oscillation period to PW and MoI is important. This is simulated for the optimal PW-MoI combinations. Figs. 9 and 10 show the sensitivity or derivatives of the oscillation period to respectively MoI and PW. Both graphs are normalized to half the oscillation period. It can clearly be seen that for a small series resistor of the switch, the impact of applying an inaccurate pulse is higher than for switches with

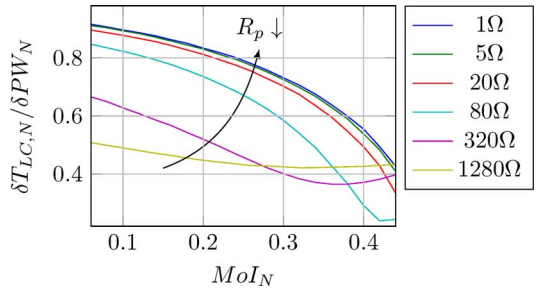

Fig. 10. Sensitivity of the oscillation period to the pulse width. The derivative is calculated for the optimal PW-MoI combinations. All axes are normalized to half the oscillation period since this is the time span in which the pulse is applied.

a high series resistance (more charge is injected in the tank). These simulated sensitivities are useful when estimating the impact of an inaccurate pulse due to changes in temperature or other external factors. It will be seen that these results correspond properly with the (simulated) ISF (Section III).

2) Estimate of the Impact of Temperature and Supply Voltage Changes: The calculation of the impact of inaccurate applied pulses is rather straightforward. Since a complete oscillation period contains one cycle which is influenced by the pulse and n free-running cycles, one oscillation period can be written as follows:

$$T_{\rm osc} = n \cdot T_{\rm LC} + T_{\rm LC} \cdot (1 + \Delta T_{{\rm LC},N}/2) \tag{10}$$

$$= (n+1) \cdot T_{\rm LC} + T_{\rm LC}/2 \cdot \frac{\Delta T_{\rm LC}}{T_{\rm LC}/2} \tag{11}$$

in which $T_{\rm osc}$ is the pulse frequency, n is the number of free-running cycles and $\Delta T_{{\rm LC},N}$ is the relative deviation of the half LC tank period due to the applied pulse. When the sensitivities of the period to MoI and PW are known, the relative impact of an inaccurate pulse on $T_{\rm osc}$ is calculated as follows:

$$\frac{\Delta T_{\rm osc}}{T_{\rm osc}} = \frac{\frac{\delta T_{\rm LC}}{\delta {\rm MoI}} \cdot \Delta{\rm MoI} + \frac{\delta T_{\rm LC}}{\delta {\rm PW}} \cdot \Delta{\rm PW}}{(n+1) \cdot T_{\rm LC}} \tag{12}$$

$$= \frac{\frac{\delta T_{{\rm LC},N}}{\delta {\rm MoI}_N} \cdot \Delta{\rm MoI}_N + \frac{\delta T_{{\rm LC},N}}{\delta {\rm PW}_N} \cdot \Delta{\rm PW}_N}{2 \cdot (n+1)} \tag{13}$$

where all the values with subscript N are normalized to half the LC tank period. From this equation it is clearly visible that the oscillation period only suffers weakly from inaccurate pulsing. From Fig. 6 it appears that this linear approach is a reasonable approximation, even for high values of $\Delta\,{\rm MoI}_N$ and $\Delta\,{\rm PW}_N$. When, for instance, PW varies over temperature with 30%, this has only an impact of around 0.5% on the frequency in case of 31 free-running cycles. A quantitative calculation of the expected temperature and supply voltage dependency is performed in Section V.D, where the implemented circuit is discussed.

III. Phase Noise Behavior of the Pulsed LC Oscillator

To describe the phase noise behavior of the pulsed LC oscillator, a distinction must be made between the two phases of the oscillation cycle. The first part is the free-running phase, which is basically a decaying LC tank. The pulsed phase, however, is somewhat more complex to describe analytically. The results from the previous section will be useful to predict the worst-case phase noise behavior.

A. Noise Injection During the Free-Running Period

The noise of the oscillator during the free-running period is closely connected to that of a harmonic LC oscillator. The main difference, however, is the decaying amplitude which has a significant influence, as will be seen. According to [7] and [8] oscillators can be described as a Linear Time Varying (LTV) system. This can easily be explained by analyzing Fig. 11. In this phase portrait of a pulsed oscillator with 15 free-running cycles, an equal charge is injected in the oscillator at two different moments. This causes a ΔV over the capacitor, which is also equal in both cases ($\Delta V_1 = \Delta V_2$). The induced phase shift, however, is different: when the charge is injected around the maximum of the output voltage, a much smaller phase shift is caused than in the case of a zero crossing. Note that this is the same conclusion as in Section II about the injection of a Dirac impulse. Furthermore, the oscillation amplitude plays an important role. The second charge is injected at a low amplitude which results in a higher induced phase shift. Since the phase of the randomly injected noise is not important [7], the sign difference between $\Delta\theta_1$ and $\Delta\theta_2$ can be neglected. To account for the time-dependent noise sensitivity, the impulse sensitivity function (ISF) was defined in [7]. This function, $\Gamma(\tau\omega_{\rm osc})$, is a dimensionless, frequency- and amplitude-independent function with period 2π which describes the induced phase shift due to an injected unit pulse at $t = \tau$. The unit impulse response for the excess phase is equal to:

$$h_\phi(t,\tau) = \frac{\Gamma(\omega_{\rm osc}\tau)}{q_{\rm max}} \cdot u(t-\tau) \tag{14}$$

where $q_{\rm max}$ is the maximum charge on the tank capacitor, which takes the amplitude into account, and $u(t)$ is the unit step. When the injected noise $i(t)$ is considered to be a sum of discrete charge injections, the output phase shift $\phi(t)$ induced by the noise can be calculated using:

$$\phi(t) = \int_{-\infty}^{+\infty} h_\phi(t,\tau) \cdot i(\tau) d\tau \tag{15}$$

$$= \frac{1}{q_{\rm max}} \cdot \int_{-\infty}^{t} \Gamma(\omega_{\rm osc}\tau) \cdot i(\tau) d\tau \tag{16}$$

To avoid any confusion, $q_{\rm max}$ is defined as the maximum charge difference on the capacitor compared to the equilibrium state, i.e., the difference charge at the first minimum after the applied pulse.

1) Calculation of the ISF: The ISF of the oscillator during the free-running cycles can be calculated analytically. In case of a second-order system, the following formula is used:

$$\Gamma_i(\omega t) = \frac{f'}{f'^2 + f''^2} \tag{17}$$

where the normalized capacitor voltage is the first state variable and its first derivative is the normalized current through the in-

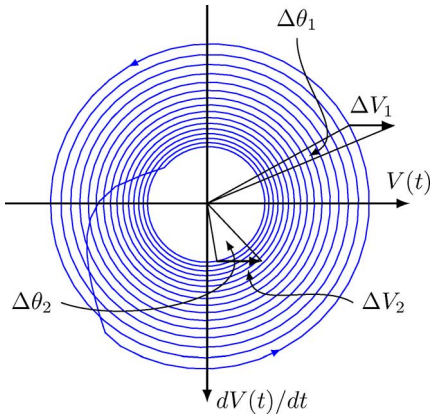

Fig. 11. State diagram of a pulsed oscillator. The LC network is similar to Fig. 5 with a switch discharging the state capacitor. An equal noise voltage ΔV is added at two different moments in the oscillation, causing a different phase shift $\Delta\theta$ in the output wave.

ductor, which is the second state variable. The ISF then results in:

$$\Gamma(x) \approx \frac{-e^{\frac{x}{2Q}} \cdot \sin\left(\frac{\sqrt{4Q^2-1}}{2Q}x + 2\theta\right)}{\frac{2Q}{\sqrt{4Q^2-1}} - \frac{2Q}{4Q^2-1}\sin\left(\frac{\sqrt{4Q^2-1}}{Q}x + 5\theta\right)} \tag{18}$$

which is independent of the oscillation amplitude and the natural angular frequency. To get a complete picture of the ISF, this result needs to be combined with the impulse sensitivity during the applied pulse.

B. ISF During the Applied Pulse

Although the curve in the state diagram of Fig. 11 can be calculated exactly for a resistive switch, the result strongly depends on the boundary conditions, i.e., the exact value of the state variables at the starting and ending point of the applied pulse. An easier, and often more accurate, calculation method is proposed in [7]: inject a unit charge at different moments during the oscillation period and measure the corresponding induced phase shift, which is proportional to the ISF.

The numerical Matlab model of Fig. 5 was used to simulate the ISF. On Fig. 12 the simulated ISF is shown together with the previously calculated ISF during the free-running period and the output waveform of the pulsed LC tank. Both calculation methods result in an almost identical waveform of the ISF. The ISF during the applied pulse is much smaller than the ISF during the free-running period. The extra noise source coming from the switch can therefore be neglected.

C. ISF of a Harmonic Oscillator

It is interesting to compare this ISF to that of a continuously driven harmonic oscillator. The calculation is rather straightforward. Since the normalized waveform is in this case equal to:

$$h_n(x) = \cos(x) \tag{19}$$

the ISF is calculated to be, using (17):

$$\Gamma(x) = -\sin(x) \tag{20}$$

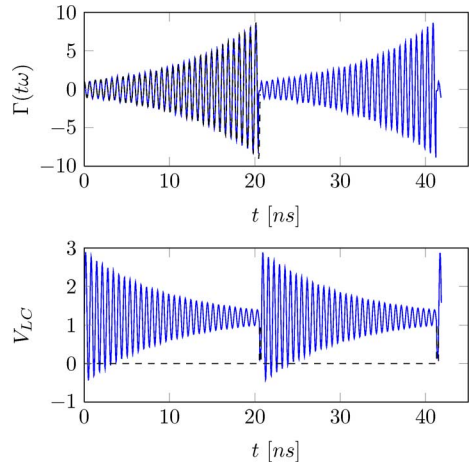

Fig. 12. (Top) The ISF of the pulsed oscillator. The blue curve is the numerically simulated ISF, the black dashed curve represents the analytically calculated ISF during the free-running period. Both curves are almost identical. (Bottom) The corresponding output waveform of the LC tank. The black dashed line shows the pulses applied to the LC tank.

It will be shown that this more symmetrical waveform leads to a better phase noise performance.

IV. Impact of the Different Noise Sources

Using the ISF, it is possible to calculate the resulting phase noise and jitter caused by the different noise sources. During the free-running period, two noise sources are identified: thermal noise from the tank and supply noise. Another strategy, based on the conclusions of the first paragraph is used to calculate the influence of the noise in the applied pulse.

A. Phase Noise in the Pulsed Oscillator

The noise in the $1/f^2$ region around the carrier is an up conversion of the white noise sources. The thermal noise in the inductor, caused by R_s is considered to be a white noise source, therefore, the $1/f^3$ contribution is neglected. The noise power spectral density of R_s is equal to:

$$\frac{\overline{v_n^2}}{\Delta f} = 4 \cdot k \cdot T \cdot R_s \tag{21}$$

where k is the Boltzmann constant and T is the absolute temperature. The noise source is in series with the inductor L (see Fig. 5). To estimate the impact of this noise source on the oscillator jitter, this source needs to be translated to a corresponding current source at the output node. This results in a current source with amplitude:

$$i_n = \frac{v_n}{R_s + s \cdot L} \tag{22}$$

As explained in [7], the phase noise is mainly determined by the noise around integer multiples of the oscillation frequency f_{osc}. The FFT of the ISF is calculated and shown in Fig. 13. The most important frequency component of the ISF is at 32 times the oscillation frequency. Therefore, the noise at this frequency is dominant and determines the phase noise of the oscillator. Using

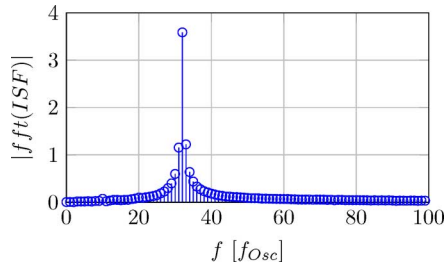

Fig. 13. Fast Fourier transform of the ISF. The most important frequency component is at $32 \cdot f_{\rm osc} = f_{\rm LC}$.

(22), the noise power spectral density at the tank's oscillation frequency is equal to:

$$\frac{\overline{i_n^2}}{\Delta f} = \frac{4kTR_sC}{L} \tag{23}$$

Exactly the same result is obtained when using the equivalent parallel resistor R_p as a noise source instead of calculating the equivalent output noise of the series resistor R_s. Next, the formula from [7], [9] to convert the white input noise into a phase noise spectrum is used:

$$\mathcal{L}\{\Delta\omega\} = 10 \cdot \log\left(\frac{\Gamma_{\rm rms}^2}{q_{\rm max}^2} \cdot \frac{\overline{i_n^2}/\Delta f}{2 \cdot \Delta\omega^2}\right). \tag{24}$$

The rms value of the ISF can be calculated using the simulated waveform or using Parseval's theorem [7], resulting in:

$$\Gamma_{\rm rms} = 2.98 \tag{25}$$

From Fig. 5 it can be seen that the also the supply noise is in series with the inductor and has the same transfer function to the output. The properties of this noise source, spectrum and amplitude, are unfortunately not known, which makes a proper estimation of its impact impossible. In the next section, based on the oscillator implementation, the resulting thermal phase noise is calculated.

B. Phase Noise in a Harmonic Oscillator

This result needs to be compared to the noise in a continuously driven oscillator. The amplitude is chosen in such a way that the averaged tank losses are the same as in the pulsed oscillator. From [3] it is known that:

$$E_{Cte}(N) = N \cdot 2 \cdot \pi \frac{V_{CT}^2 \cdot C}{2 \cdot Q} \tag{26}$$

for a continuously driven tank, and:

$$E_{\rm Decay}(N) = \frac{V_A^2 \cdot C}{2}\left(1 - e^{\frac{-2\pi N}{Q\sqrt{1-1/4Q^2}}}\right) \tag{27}$$

for the pulsed tank. This makes:

$$\frac{q_{Cte}}{q_{\rm Pulsed}} = \frac{V_{Cte}}{V_{\rm Pulsed}} \tag{28}$$

$$= \sqrt{Q \cdot \frac{1 - e^{\frac{-2\pi N}{Q\sqrt{1-1/4Q^2}}}}{2 \cdot \pi \cdot N}} = 0.47 \tag{29}$$

The numerical results are found in Section V.

V. Implementation of the Pulsed LC Oscillator

In this section the results of the previous sections are applied to a real implementation of a pulsed harmonic oscillator.

A. Design of the LC Tank

A high Q factor means that the losses in the tank are low, which improves the energy dissipation of the oscillator as well as the noise performance of the oscillator (18). Integrated inductors are typically built in the higher, more conductive metal layers, but even then the series resistance is considerable. Furthermore, the silicon substrate acts as a ground plane or mirror for the current in the inductor and therefore affects the inductance [5]. Due to the Eddy currents in the substrate, the energy losses and series resistance increase drastically. When a bondwire inductor is used instead, these effects can be diminished. According to (3), the Q factor of the tank is increased by using a larger inductor and a smaller capacitor for the same natural frequency. The limit to the inductor size in integrated applications is the available chip area. As shown in [5], the inductance and series resistance can be calculated by hand; however, finite element simulations using FastHenry show results which are more accurate [10]. These simulations of the integrated LC tank using a 1750 μm × 1500 μm bondwire inductor and MiM capacitors result in the following tank properties [3]:

$$\begin{array}{ll} L = 30.4\ \text{nH} & C = 351\ \text{fF} \\ R_s = 6.48\ \Omega & Q = 45.4 \\ \omega_n = 9.651\ \text{Grad/s} & = 2\pi 1.54\ \text{GHz} \end{array} \tag{30}$$

In these simulations, the influence of a 300 μm thick, highly doped substrate is taken into account. This is expected to be an overestimate of the real substrate losses.

1) Resulting Noise During the Free-Running Period: For $V_{\rm DD} = 1.6$ V, the maximum charge in the tank is equal to:

$$q_{\rm max} = V_{\rm DD} \cdot C = 5.62e{-}13\ \text{C} \tag{31}$$

$$k = 1.38e{-}23\ \text{m}^2\ \text{kg/s}^2\ \text{/K} \tag{32}$$

At room temperature the estimated phase noise close to the output frequency is then equal to:

$$\mathcal{L}\{\Delta\omega\}_{\rm dB} = 10 \cdot \log\left(\frac{17.44}{\Delta\omega^2}\right) \tag{33}$$

To translate this to the jitter on the oscillator output signal, the following formula can be used [11]:

$$\sigma_{\rm LC} = \sqrt{\frac{\Delta f^2 \cdot \mathcal{L}\{\Delta f\}}{f_{\rm osc}^3}} = 1.10e{-}14 \tag{34}$$

To obtain the jitter on the total oscillation period (which contains 32 tank cycles), the standard deviation needs to be multiplied by $\sqrt{32}$, resulting in:

$$\sigma_{\rm osc} = 6.22e{-}14\ \text{s} \tag{35}$$

2) Resulting Noise in the Harmonic Oscillator: The maximum charge in the circuit is, according to (29) equal to $2.65e-13$ C. Since the tank itself is the same in both cases, the injected noise current is also assumed to be the same. Using (24) and (34) this results in a tank jitter of:

$$\sigma_{\rm tank} = 5.52e{-}15\ \text{s} \tag{36}$$

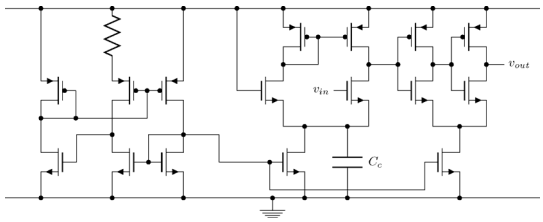

Fig. 14. The amplifier used to detect the LC output signal is a differential pair in combination with 2 CMOS inverters. The differential pair is shown (right) together with the supply-independent biasing circuit (left).

Although the maximum charge in the tank is a factor of two lower than in the first case (see IV.B), the jitter is also much lower. This is caused by the irregular waveform of the ISF, which results in a higher rms value and therefore also a high noise sensitivity. In [12] it is shown that in a well-designed oscillator the noise added by the active devices in in the same order of magnitude. Due to the high-Q tank, a good noise performance is therefore expected.

B. Design of the Differential Amplifier

The smaller the signals the amplifier can detect, the more oscillation periods the tank can be free-running. The chosen topology for the amplifier is a differential pair in combination with two differentially biased CMOS inverters as shown in Fig. 14. Since the input signal of the amplifier is not differential, an extra capacitor C_c connects the source of the differential transistors to the ground. In this way the gain is large at high frequencies without losing the self-biasing benefits of a differential pair at DC. As will be seen, the output signal does not have to be rail to rail to trigger the clock input of the TSPC flip-flops which also reduces the power consumption drastically. To make the behavior of the amplifier independent of the supply voltage, the biasing circuit shown on the left-hand-side of Fig. 14 is used [13]. This circuit keeps the current through the differential pair constant at different supply voltages. In Fig. 15 the delay and peak-to-peak output signal is shown as a function of the input amplitude. For a falling edge at the input (to trigger the counter), the delay increases because the first stage slews. Rising edges cause a quick discharge of the first stage's output into C_c, which increases the speed of the critical path (see V.D1). This, however, has no impact at low amplitudes, when the tank is pulsed. A last measure to decrease the power consumption is by reducing the left side of the differential pair. The total current consumption of the amplifier is then around 10 μA when a 30 mV tank amplitude can be detected.

C. The Counter

The ripple counter is built out of 5 TSPC Flip-Flops. The schematic of the used flip-flop is shown in Fig. 16. The steepness of the applied clock flank to the flip-flop is crucial to prevent it from data-loss or ripple-through. This, however, does not pose any problem using the 1.5 GHz tank output. Different measures were taken to reduce the power consumption of the counter. One of them is the addition of a current source at the ground node, which limits the current at high supply voltages. Furthermore, due to the resulting ground lift, the clock at the input does not need to be rail-to-rail. The resulting power consumption is below 10 μW at 1.1 V.

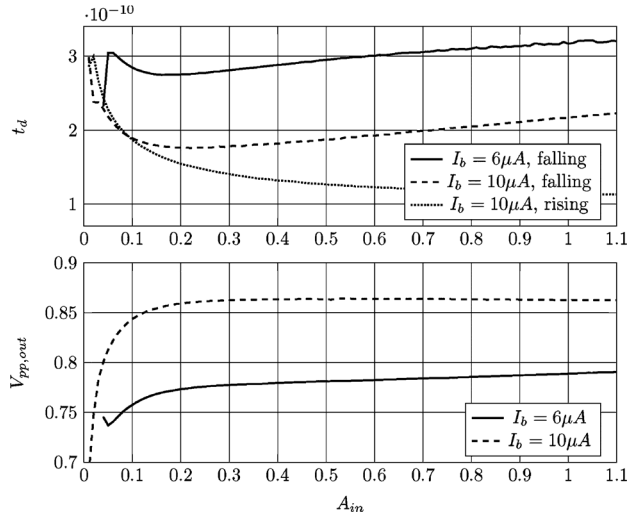

Fig. 15. Delay and peak-to-peak output signal for different input amplitudes at $V_{\mathrm{DD}} = 1.1$ V and for a falling and a rising edge at the input. The circuit is able to detect a 10 mV signal when the biasing current is 10 μA. When the current is decreased, the sensitivity also decreases.

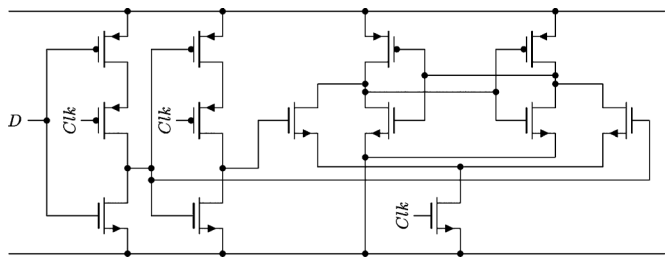

Fig. 16. The ripple counter is built out of 5 TSPC Flip-Flops.

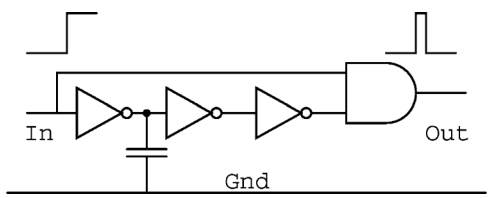

Fig. 17. The pulse width of the Pulse Generator is controlled by the inverter delay in combination with the output capacitor.

D. The Pulse Generator

As shown previously, PW as well as MoI have an influence on the zero crossings of the LC-tank's output voltage. The delay to control PW is controlled by a chain of differentially biased inverters and a capacitor at the output of the first inverter. This is shown in Fig. 17. The combination of inverters is very similar to the structure of the previously discussed amplifier. The use of current sources allows the pulse generator to be switched-off most of the time and makes PW stable under a changing supply voltage and temperature. The biasing circuit shown in Fig. 14 is shared between the inverters and the differential amplifier. Due to process variations, it is difficult to predict the precise series resistance of the NMOS switch which has to discharge the tank's capacitor. Therefore, the capacitor is sized to generate a pulse of 30% of the oscillation period. From Fig. 8 appears that at this PW, the curves of optimal MoI-PW combinations for different switch resistances cross each other. Furthermore, from Figs. 9 and 10 the sensitivity to both the MoI and the PW are rather constant and have therefore no important impact on the chosen PW. This PW is long enough to completely discharge the

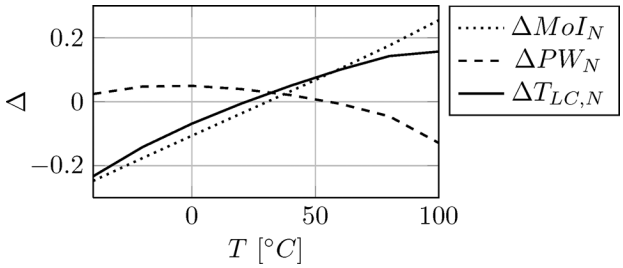

Fig. 18. Impact of the changing temperature on the output PW and MoI. The combined impact on the pulsed period is also shown.

capacitor and to result in a maximum amplitude almost equal to the supply voltage (see Fig. 7).

1) The Influence of Inaccurate Pulses: For the implemented 1.54 GHz tank, the desired optimal PW is around 195 ps. This value corresponds to a MoI of 81 ps after the zero crossing of the tank output signal. Unfortunately, in the used technology (130 nm CMOS), keeping the critical path between the tank and the output of the pulse generator lower than 100 ps is a real challenge. According to [14], in 130 nm CMOS, inverter delays are in the order of magnitude of 20 ps to 30 ps. Therefore, the pulse generator is not triggered by the falling edge, but by the preceding rising edge of the tank's output signal. In this way, the total delay of the critical path is designed to be 414 ps. This of course has a significant drawback relating the accuracy of MoI: temperature and voltage variations have a constant relative impact on the delay of the critical path. In absolute numbers, this will have a 5 times higher impact on the MoI than in the case the pulse was triggered by the corresponding falling edge!

Circuit simulations were performed to estimate the variation on the PW and the MoI over temperature and supply voltage. From Figs. 9 and 10 the worst case relative sensitivities of the MoI and the PW are estimated to be 1.02 and 0.8 respectively. These simulation results are shown in Fig. 18 together with the impact on the pulsed oscillation period. Similar simulations were performed to estimate the impact of the supply voltage. From (13) it appears that $\Delta T_{\mathrm{LC},N}$ must be divided by two times the number of free-running cycles to obtain the temperature and supply voltage sensitivity of T_{osc}:

$$T_{\mathrm{Sens}} = 43.6\ \mathrm{ppm/^{\circ}C} \tag{37}$$

$$V_{\mathrm{Sens}} = 59.2\ \mathrm{ppm/V} \tag{38}$$

This deviation is mainly determined by the variation of MoI which is much higher than the variation of PW.

2) Noise in the Pulse Generator: To calculate the noise on the injected pulses, transient noise simulations were performed. The noise in the pulse generator but also the noise generated in the amplifier have an influence on MoI and/or PW. Hence, both circuits were connected to each other, with an ideal sine wave at the input which simulates the tank's output signal. The variation of MoI as well as PW were monitored over 10000 iterations. It appears that the noise on both output variables is uncorrelated. When taking a closer look at the pulse generator topology, this can be expected indeed. When the output values of PW and MoI are analyzed, both values have a normal distribution. Using again the worst-case sensitivities of MoI and PW, and using (13) the relative standard deviation on the zero crossing of the pulsed T_{LC} and of T_{osc} is calculated to be:

$$\sigma_{\mathrm{LC,Pulsed},N} = 0.0069 \tag{39}$$

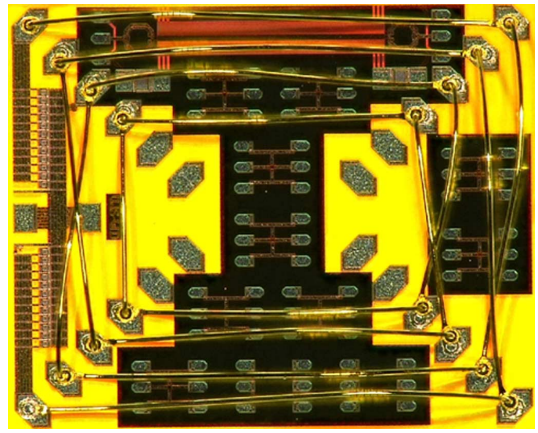

Fig. 19. Microphotograph of the pulsed LC oscillator. Some other unrelated test circuitry is laid out under the inductor.

TABLE I
OVERVIEW OF THE KEY PROPERTIES (12 SAMPLES)

Technology	130 nm CMOS
Area	1750 μm by 1500 μm
Power consumption at 1.1 V	46 μW
Max. Temp. Coefficient (-40 to 100 °C)	92 ppm/°C
Max. Voltage Coefficient (0.6 to 1.6 V)	74 ppm/V
Frequency	47.3 MHz
Abs. Accuracy (σ, Automatically bonded)	0.76% (359 KHz)

$$\sigma_{\mathrm{osc}}/T_{\mathrm{osc}} = 1.08 \times 10^{-4} \tag{40}$$

$$\sigma_{\mathrm{osc}} = 2.29e{-}12\ \mathrm{s} \tag{41}$$

These values clearly show that the noise in the pulse generator is several orders of magnitude higher than the tank noise (35). When simulating the jitter of the complete oscillator (including biasing circuitry etc.), similar figures are obtained: $3.60e{-}12$ s for the applied pulses and $4.14e{-}12$ s at the low-frequency output of the counter, which is *not* in the critical path. However, as a result of the single-ended structure of the implemented oscillator, the circuitry is vulnerable to supply noise, which is discussed in the next section.

VI. MEASUREMENT RESULTS

The key properties of the oscillator are listed in Table I and a chip photograph is shown in Fig. 19. The large chip area is an important drawback of bondwire inductors. However, as can be seen on the chip photograph, other circuitry can be laid out under the inductor. Furthermore, at higher frequencies, this technique can also be used with high-Q monolithic inductors. Figs. 20 and 21 show the output frequency as a function of temperature and supply voltage respectively. Both the measured temperature and supply voltage sensitivity are similar to the predictions of Section V.D1. The difference between measurements and simulations are likely caused by the fact that no temperature dependency was modeled in the inductor. When the number of free running cycles is lowered, lower supply voltages can be used. This however, has a negative impact on the temperature and voltage behavior. The minimum measured power consumption at 1.1 V is equal to 46 μW. Using (27) the power losses in the tank are estimated to be 10 μW; almost the same amount of energy is lost in the NMOS switch. The remaining 26 μW

TABLE II
COMPARISON TO THE STATE OF THE ART

Ref.	Tech. [μm]	Oscillator	f [MHz]	T Sens. [ppm/°C]	V Sens. [ppm/V]	P [μW]	V-Range [V]	Rel. V-Range [%]*	Trimming/ Calibration
This Work	0.13	pulsed harmonic	47.3	**92**	**74**	**46**	**0.6 – 1.6**	**91**	no
[2], ESSCIRC09	0.13	harmonic, RC	24	-	**104**	**33**	**0.4 – 1.4**	**111**	no
[4], JSSC09	65nm	harmonic, RC	6	**86**	-	**66**	1.08 – 1.32	20	no
[15], ISSCC09	0.18	relaxation, RC	14	**107**	16e3	**43**	1.7 – 1.9	22	no
[16], SBCCI03	0.5	relaxation, RC	12.8	625	5.3e3	> 400	**2.5 – 5.5**	**75**	yes
[17], JSSC07	0.35	harmonic, LC	12	**12**	**38**	31mW	4.5 – 5.5	20	yes
[18], JSSC06	0.25	ring	7	**315**	8.8e3	1.5mW	2.4 – 2.75	14	no

* $\Delta V_{rel} = 2 \cdot (V_{max} - V_{min})/(V_{max} + V_{min}) \cdot 100\%$

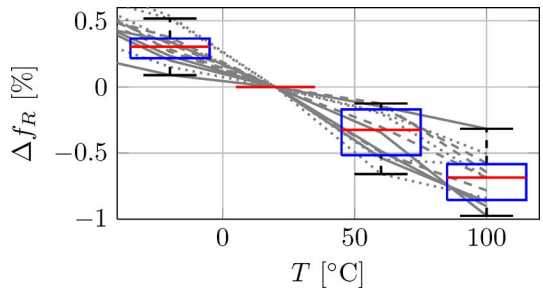

Fig. 20. Measured relative frequency error of the twelve measured samples. As predicted in Section V.D1, the frequency drops with increasing temperature.

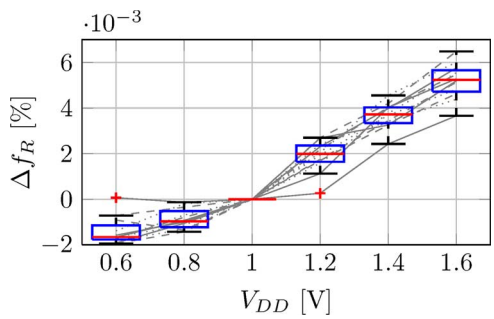

Fig. 21. Measured relative frequency error over different supply voltages.

is consumed in the oscillator circuit. The power consumption of the circuitry increases almost linearly up to 79 μW at 1.6 V. Due to the amplitude dependence of the amplifier delay, the duty cycle of the different outputs of the counter is not equal to 0.5 and is slightly beating in some outputs. This causes spurious in the spectrum of the higher frequency outputs. The measured output jitter is 12 to 15 times higher as the simulated value. In Fig. 22 the histogram of the measured output jitter is shown. The two peaks are most likely caused by supply and/or substrate coupling of the unused (but switching) sixth bit of the counter and its output buffers. This extra bit is present for testing reasons in this prototype. Simulation results with and without this coupling are also shown in Fig. 22 and fit quite well with the measurements. It is therefore assumed that supply coupling is the main reason for the decreased noise performance. An extensive supply decoupling and/or a more optimized differential structure are needed to overcome this artifact. A comparison to the state of the art is shown in Table II. Only the LC oscillator presented in [17] has a better temperature and voltage behavior, be it at the cost of a high power consumption. The proposed topology is a stable, low-power oscillator alternative that can be used over a wide voltage and temperature range.

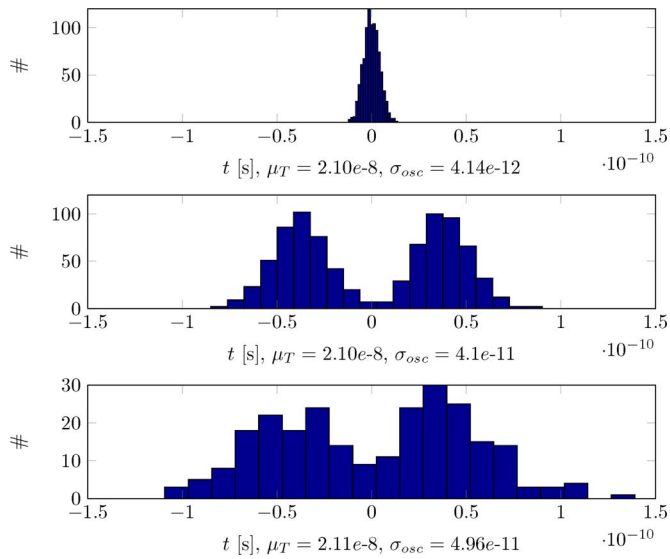

Fig. 22. Output jitter of the oscillator. The upper plot shows the simulated jitter, without supply noise. In the second plot, supply noise is added to simulate the noise injection of the digital circuitry and thermal noise to match the measured output jitter, which is shown in the lower plot.

VII. CONCLUSION

A pulsed oscillator topology based on an LC tank has been analyzed. Due to the the high-Q LC tank and the pulsed driving technique, the oscillator has a low power consumption compared to other integrated LC oscillators. Furthermore, a low supply voltage dependency of 74 ppm/V and a temperature dependency of 92 ppm/°C are obtained over a wide supply and temperature range. The impact of the oscillator circuitry on the frequency stability and output noise was discussed elaborately. It was shown that the irregular waveform results in an increase of the noise sensitivity. The intrinsic noise of the oscillator is dominated by pulse generator, however, in this single-ended implementation it is the supply noise which degrades the performance. This can drastically be improved using a differential structure and/or better supply decoupling. The power consumption at 1.1 V is 46 μW, which makes the pulsed oscillator suited for applications such as autonomous sensor networks, requiring low energy consumption.

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